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Substitute for Form PTO-1449				<i>Complete if known</i>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>O I P E</i> (use as many sheets as necessary)				Application Number	09/691,406
				Filing Date	October 17, 2000
				First Named Inventor	Christopher Hoover
				Group Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	1	of	1	Attorney Docket Number	21891.02500

APR 10 2002

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant Of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
\$	A1	5,963,447		Kohn et al.	10/05/1999

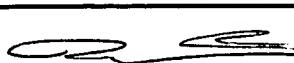
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FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Office ³	Number ⁴	Kind Code ⁵ (if known)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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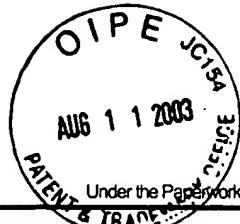
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			
\$	C1	Rogers, P. et al. (1997) "A Simulation Testbed for Comparing the Performance of Alternative Control Architectures," <i>Proceedings of the 1997 Winter Simulation Conference</i> , pp. 880-887			
\$	C2	Oreizy, P. et al. (1999) "An Architecture-Based Approach to Self-Adaptive Software," <i>IEEE Intelligent Systems</i> , 14(3):54-62			
\$	C3	Clarke, P. (1999) "Cadence Virtual Component Codesign Tools Set for January Release," <i>Electronic Engineering Times</i> , 1087:80			
\$	C4	Santarini, M. (2000) "Cadence Rolls System-Level Design to Fore," <i>Electronic Engineering Times</i> , 1095:pp. 1, 22, 24 and 130			

Examiner Signature		Date Considered	03/31/2005
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation is not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

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PTO/SB/08b(05-03)

Approved for use through 04/30/2003. OMB 0651-0031

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Substitute for Form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1

of

1

Complete if Known

Application Number	09/691,406
Filing Date	October 17, 2000
First Named Inventor	Christopher Hoover
Group Art Unit	2123
Examiner Name	Not assigned

Attorney Docket Number 21891.02500

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
\$ /	AA	CASSAGNOL, BOB; et al., "Codesigning a Complex System on a Chip with Behavioral Models," November 1998, http://2www.isdmag.com/Editorial/1998/coverstory9811.html , 3/18/00.	
\$ /	AB	Cadence website, Cadence Press Release, "Addressing the Systems-in-Silicon Verification Challenge," http://www.cadence.com/press_box/na/pr/1995/inca.html , 3/18/00	RECEIVED
\$ /	AC	Cadence website, "System-Level design," http://www.cadence.com/technology/hwsw/vcc/html , 3/18/00	AUG 12 2003
\$ /	AD	Cadence website, "System-Level design," http://www.cadence.com/technology/hwsw/ , 3/18/00	Technology Center 2100
\$ /	AE	Cadence website, "Digital Block Implementation," http://www.cadence.com/technology/digital/ , 3/18/00	
\$ /	AF	Cadence website, "Functional Design and Verification," http://www.cadence.com/technology/funct/ , 3/18/00	
\$ /	AG	Cadence website, "Custom Block Implementation," http://www.cadence.com/technology/custom/ , 3/18/00	
\$ /	AH	Cadence website, "Physical Verification, Extraction and Analysis," http://www.cadence.com/technology/phys/ , 3/18/00	
\$ /	AI	Cadence website, "Chip Planning and Assembly," http://www.cadence.com/technology/chip/ , 3/18/00	
\$ /	AJ	Cadence website, "PCB Design and IC Packaging," http://www.cadence.com/technology/pcb , 3/18/00	
\$ /	AK	WILSON, LES and CRITTEN, JEFF, "White Paper: DSP SOC Design Methodology for Digital Camera," 2000, Cadence Design Systems, Inc.	

Examiner Signature		Date Considered	03/31/2006
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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